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The *Lift* Project: Performance Portable Parallel Code Generation via Rewrite Rules

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http://www.lift-project.org/





What are the problems *Lift* tries to tackle?

- Parallel processors everywhere
- Many different types: CPUs, GPUs, ...
- Parallel programming is hard
- Optimising is even harder
- **Problem**: No portability of performance!



Reduction Case Study

- Optimising OpenCL is complex
 - Understanding of target hardware required
- Program changes not obvious
- Is it worth it? ...

```
kernel
void reduce0(global float* g_idata,
             global float* g odata,
            unsigned int n,
            local float* l data) {
 unsigned int tid = get local id(0);
 unsigned int i = get_global_id(0);
 l_data[tid] = (i < n) ? g_idata[i] : 0;
 barrier(CLK LOCAL MEM FENCE);
 for (unsigned int s=1;
      s < get local size(0); s = 2 {
   if ((tid % (2*s)) == 0) {
     l data[tid] += l data[tid + s];
   barrier(CLK_LOCAL_MEM_FENCE);
  }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
 unsigned int tid = get_local_id(0);
 unsigned int i =
   get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
    WG SIZE * get_num_groups(0);
 l_data[tid] = 0;
 while (i < n) {
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l data[tid] += l data[tid+128]; }
   barrier(CLK LOCAL MEM FENCE); }
 if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

Performance Results Nvidia



(a) Nvidia's GTX 480 GPU.

- ... Yes! Optimising improves performance by a factor of 10!
- Optimising is important, but ...

Performance Results AMD and Intel



- ... unfortunately, optimisations in OpenCL are not portable!
- **Challenge**: how to achieving portable performance?

Lift: Performance Portable GPU Code Generation via Rewrite Rules



• Ambition: automatic generation of Performance Portable code

Walkthrough

```
) sum(vec) = reduce(+, 0, vec)
```

rewrite rules code generation

```
2
```

```
\begin{aligned} \operatorname{vecSum} &= \operatorname{reduce} \circ \operatorname{join} \circ \operatorname{map-workgroup} \left( \\ \operatorname{join} \circ \operatorname{toGlobal} (\operatorname{map-local} (\operatorname{map-seq} \operatorname{id})) \circ \operatorname{split} 1 \circ \\ \operatorname{join} \circ \operatorname{map-warp} \left( \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 1 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 2 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 4 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 8 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 16 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 32 \\ \right) \circ \operatorname{split} 64 \circ \\ \operatorname{join} \circ \operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 64 \circ \\ \operatorname{join} \circ \operatorname{toLocal} (\operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0)) \circ \\ \operatorname{split} (\operatorname{blockSize}/128) \circ \operatorname{reorder-stride} 128 \\ \right) \circ \operatorname{split} \operatorname{blockSize} \end{aligned}
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

3

Walkthrough

```
) sum(vec) = reduce(+, 0, vec)
```

rewrite rules code generation

```
vecSum = reduce \circ join \circ map-workgroup (
join \circ toGlobal (map-local (map-seq id)) \circ split 1 \circ
join \circ map-warp (
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 1 \circ
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 2 \circ
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 4 \circ
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 8 \circ
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 16 \circ
join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 32
) \circ split 64 \circ
join \circ map-local (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 64 \circ
join \circ toLocal (map-local (reduce-seq (+) 0)) \circ
split (blockSize/128) \circ reorder-stride 128
) \circ split blockSize
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get local id(0);
  unsigned int i =
    get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
  l_data[tid] = 0;
 while (i < n) {</pre>
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
  if (WG_SIZE >= 256) {
   if (tid < 128) {
      l data[tid] += l data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
   if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

1 Algorithmic Primitives (a.k.a. algorithmic skeletons)

map(f, x):	$\begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 & x_7 & x_8 \end{bmatrix}$	$\longmapsto f(x_1) f(x_2) f(x_3) f(x_4) f(x_5) f(x_6) f(x_7) f(x_8)$
zip(x, y):	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto (x_{1,}y_{1})(x_{2,}y_{2})(x_{3,}y_{3})(x_{4,}y_{4})(x_{5,}y_{5})(x_{6,}y_{6})(x_{7,}y_{7})(x_{8,}y_{8})$
reduce(+, 0, x):	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto \qquad x_1 + x_2 + x_3 + x_4 + x_5 + x_6 + x_7 + x_8$
<pre>split(n, x):</pre>	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto \qquad \boxed{x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8}$
join(x):	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto \qquad \qquad$
iterate(f, n, x):	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto f(\dots f(x_1 x_2 x_3 x_4 x_5 x_6 x_7 x_8)\dots)$
reorder(σ , x):	$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$\longmapsto \qquad \qquad$

1 High-Level Programs

scal(a, vec) = map($\lambda x \mapsto x*a$, vec)

asum(vec) = reduce(+, 0, map(abs, vec))

dotProduct(x, y) = reduce(+, 0, map(*, zip(x, y)))

Walkthrough

```
) sum(vec) = reduce(+, 0, vec)
```

rewrite rules code generation

```
2
```

```
\begin{aligned} \operatorname{vecSum} &= \operatorname{reduce} \circ \operatorname{join} \circ \operatorname{map-workgroup} \left( \\ \operatorname{join} \circ \operatorname{toGlobal} (\operatorname{map-local} (\operatorname{map-seq} \operatorname{id})) \circ \operatorname{split} 1 \circ \\ \operatorname{join} \circ \operatorname{map-warp} \left( \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 1 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 2 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 4 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 8 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 16 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 32 \\ \right) \circ \operatorname{split} 64 \circ \\ \operatorname{join} \circ \operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 64 \circ \\ \operatorname{join} \circ \operatorname{toLocal} (\operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0)) \circ \\ \operatorname{split} (\operatorname{blockSize}/128) \circ \operatorname{reorder-stride} 128 \\ \right) \circ \operatorname{split} \operatorname{blockSize} \end{aligned}
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get_local_id(0);
  unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
  while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
   if (WG_SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

3

Walkthrough

) sum(vec) = reduce(+, 0, vec)

rewrite rules code generation

(2)

```
\begin{aligned} \operatorname{vecSum} &= \operatorname{reduce} \circ \operatorname{join} \circ \operatorname{map-workgroup} \left( \\ \operatorname{join} \circ \operatorname{toGlobal} (\operatorname{map-local} (\operatorname{map-seq} \operatorname{id})) \circ \operatorname{split} 1 \circ \\ \operatorname{join} \circ \operatorname{map-warp} \left( \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 1 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 2 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 4 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 8 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 16 \circ \\ \operatorname{join} \circ \operatorname{map-lane} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 32 \end{array} \right) \\ \circ \operatorname{split} 64 \circ \\ \operatorname{join} \circ \operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0) \circ \operatorname{split} 2 \circ \operatorname{reorder-stride} 64 \circ \\ \operatorname{join} \circ \operatorname{map-local} (\operatorname{reduce-seq} (+) \ 0) \circ \\ \operatorname{split} (\operatorname{blockSize}/128) \circ \operatorname{reorder-stride} 128 \\ ) \circ \operatorname{split} \operatorname{blockSize} \end{aligned}
```

```
kernel
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
  unsigned int tid = get local id(0);
  unsigned int i =
    get group id(0) * (get local size(0)*2)
                    + get_local_id(0);
  unsigned int gridSize =
   WG SIZE * get num groups(0);
  l_data[tid] = 0;
 while (i < n) {</pre>
   l data[tid] += g idata[i];
   if (i + WG SIZE < n)</pre>
     l data[tid] += g idata[i+WG SIZE];
   i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
   if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
    barrier(CLK LOCAL MEM FENCE); }
  if (WG_SIZE >= 128) {
   if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
    barrier(CLK_LOCAL_MEM_FENCE); }
  if (tid < 32) {
   if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
   if (WG SIZE >= 32) {
      l data[tid] += l data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
      l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
  if (tid == 0)
   g_odata[get_group_id(0)] = l_data[0];
```

② Algorithmic Rewrite Rules

- **Provably correct** rewrite rules
- Express algorithmic implementation choices

Split-join rule:

 $map \ f \to join \circ map \ (map \ f) \circ split \ n$

Map fusion rule: $map \ f \circ map \ g \to map \ (f \circ g)$

Reduce rules:

reduce $f \ z \to reduce \ f \ z \circ reducePart \ f \ z$ reducePart $f \ z \to reducePart \ f \ z \circ reorder$ reducePart $f \ z \to join \ \circ map \ (reducePart \ f \ z) \circ split \ n$ reducePart $f \ z \to iterate \ n \ (reducePart \ f \ z)$



Primitive

OpenCL concept

mapGlobal mapWorkgroup mapLocal Work-items

Work-groups

Oper	CL thre	ad hierarchy
workg	roups	global threads
local th	nreads	

```
mapSeq
reduceSeq
```

Sequential implementations

toLocal, toGlobal Memory areas

mapVec,
splitVec, joinVec

Vectorisation

2 OpenCL Rewrite Rules

• Express low-level implementation and optimisation choices

Map rules:

 $map \ f \to map \textit{Workgroup} \ f \ | \ map \textit{Local} \ f \ | \ map \textit{Global} \ f \ | \ map \textit{Seq} \ f$

Local/ global memory rules: $mapLocal f \rightarrow toLocal (mapLocal f)$

 $mapLocal \ f \to to Global \ (mapLocal \ f)$

Vectorisation rule:

 $map \ f \to join \operatorname{Vec} \circ map \ (map \operatorname{Vec} \ f) \circ split \operatorname{Vec} \ n$

Fusion rule:

 $reduceSeq \ f \ z \circ mapSeq \ g \rightarrow reduceSeq \ (\lambda \ (acc, x). \ f \ (acc, g \ x)) \ z$

```
kernel
                   Walkthrough
                                                                              3
                                                                                    void reduce6(global float* g_idata,
                                                                                                   global float* g_odata,
                                                                                                   unsigned int n,
                                                                                                   local volatile float* l data) {
            vecSum = reduce (+) 0
                                                                                      unsigned int tid = get_local_id(0);
                                                                                      unsigned int i =
                                                                                        get_group_id(0) * (get_local_size(0)*2)
                                                                                                           + get_local_id(0);
                                                                                      unsigned int gridSize =
                                                                                        WG_SIZE * get_num_groups(0);
                                                                                      l_data[tid] = 0;
                                      code generation
  rewrite rules
                                                                                      while (i < n) {
                                                                                        l data[tid] += g idata[i];
                                                                                         if (i + WG SIZE < n)</pre>
                                                                                           l_data[tid] += g_idata[i+WG_SIZE];
                                                                                         i += gridSize; }
                                                                                      barrier(CLK_LOCAL_MEM_FENCE);
                                                                                      if (WG_SIZE >= 256) {
                                                                                        if (tid < 128) {
vecSum = reduce \circ join \circ map-workgroup
                                                                                           l_data[tid] += l_data[tid+128]; }
     join \circ toGlobal (map-local (map-seq id)) \circ split 1 \circ
                                                                                         barrier(CLK LOCAL MEM FENCE); }
     join o map-warp (
                                                                                      if (WG_SIZE >= 128) {
        join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 1 \circ
                                                                                         if (tid < 64) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 2 \circ
                                                                                           l data[tid] += l data[tid+ 64]; }
                                                                                        barrier(CLK_LOCAL_MEM_FENCE); }
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 4 \circ
                                                                                      if (tid < 32) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 8 \circ
                                                                                         if (WG SIZE >= 64) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 16 \circ
                                                                                           l_data[tid] += l_data[tid+32]; }
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 32
                                                                                         if (WG SIZE >= 32) {
     ) \circ split 64 \circ
                                                                                           l_data[tid] += l_data[tid+16]; }
     join \circ map-local (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 64 \circ
                                                                                         if (WG SIZE >= 16) {
     join \circ toLocal (map-local (reduce-seq (+) 0)) \circ
                                                                                           l_data[tid] += l_data[tid+ 8]; }
     split (blockSize/128) o reorder-stride 128
                                                                                         if (WG SIZE >= 8) {
                                                                                           l_data[tid] += l_data[tid+ 4]; }
  ) o split blockSize
                                                                                         if (WG SIZE >= 4) {
                                                                                           l_data[tid] += l_data[tid+ 2]; }
                                                                                         if (WG SIZE >= 2) {
```

```
24
```

l_data[tid] += l_data[tid+ 1]; } }

g_odata[get_group_id(0)] = l_data[0];

if (tid == 0)

```
kernel
                     Walkthrough
                                                                                        3
             vecSum = reduce (+) 0
   rewrite rules code generation
vecSum = reduce \circ join \circ map-workgroup
      join \circ toGlobal (map-local (map-seq id)) \circ split 1 \circ
      join o map-warp (
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 1 \circ
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 2 \circ
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 4 \circ
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 8 \circ
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 16 \circ
         join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 32
      \circ split 64 \circ
      join \circ map-local (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 64 \circ
      join \circ toLocal (map-local (reduce-seg (+) 0)) \circ
      split (blockSize/128) o reorder-stride 128
   ) • split blockSize
```

```
void reduce6(global float* g_idata,
             global float* g_odata,
             unsigned int n,
             local volatile float* l data) {
 unsigned int tid = get_local_id(0);
 unsigned int i =
   get_group_id(0) * (get_local_size(0)*2)
                    + get_local_id(0);
 unsigned int gridSize =
   WG_SIZE * get_num_groups(0);
 l_data[tid] = 0;
 while (i < n) {
   l data[tid] += g idata[i];
    if (i + WG SIZE < n)</pre>
     l_data[tid] += g_idata[i+WG_SIZE];
    i += gridSize; }
  barrier(CLK_LOCAL_MEM_FENCE);
 if (WG_SIZE >= 256) {
    if (tid < 128) {
     l_data[tid] += l_data[tid+128]; }
   barrier(CLK LOCAL MEM FENCE); }
 if (WG_SIZE >= 128) {
    if (tid < 64) {
     l data[tid] += l data[tid+ 64]; }
   barrier(CLK_LOCAL_MEM_FENCE); }
 if (tid < 32) {
    if (WG SIZE >= 64) {
     l_data[tid] += l_data[tid+32]; }
    if (WG SIZE >= 32) {
     l_data[tid] += l_data[tid+16]; }
    if (WG SIZE >= 16) {
     l_data[tid] += l_data[tid+ 8]; }
    if (WG SIZE >= 8) {
     l_data[tid] += l_data[tid+ 4]; }
    if (WG SIZE >= 4) {
     l_data[tid] += l_data[tid+ 2]; }
    if (WG SIZE >= 2) {
     l_data[tid] += l_data[tid+ 1]; } }
 if (tid == 0)
    g_odata[get_group_id(0)] = l_data[0];
```

③ Pattern based OpenCL Code Generation

Generate OpenCL code for each OpenCL primitive

$$mapGlobal \ f \ xs$$
 —

for (int g_id = get_global_id(0); g_id < n;
 g_id += get_global_size(0)) {
 output[g_id] = f(xs[g_id]);
}</pre>

 $reduceSeq \ f \ z \ xs \ \longrightarrow$

 A lot more details about the code generation implementation can be found in our <u>CGO 2017 paper</u>

```
kernel
                   Walkthrough
                                                                              3
                                                                                    void reduce6(global float* g_idata,
                                                                                                   global float* g_odata,
                                                                                                   unsigned int n,
                                                                                                   local volatile float* l data) {
            vecSum = reduce (+) 0
                                                                                      unsigned int tid = get_local_id(0);
                                                                                      unsigned int i =
                                                                                        get_group_id(0) * (get_local_size(0)*2)
                                                                                                           + get_local_id(0);
                                                                                      unsigned int gridSize =
                                                                                        WG_SIZE * get_num_groups(0);
                                                                                      l_data[tid] = 0;
                                      code generation
  rewrite rules
                                                                                      while (i < n) {
                                                                                        l data[tid] += g idata[i];
                                                                                         if (i + WG SIZE < n)</pre>
                                                                                           l_data[tid] += g_idata[i+WG_SIZE];
                                                                                         i += gridSize; }
                                                                                      barrier(CLK_LOCAL_MEM_FENCE);
                                                                                      if (WG_SIZE >= 256) {
                                                                                        if (tid < 128) {
vecSum = reduce \circ join \circ map-workgroup
                                                                                           l_data[tid] += l_data[tid+128]; }
     join \circ toGlobal (map-local (map-seq id)) \circ split 1 \circ
                                                                                         barrier(CLK LOCAL MEM FENCE); }
     join o map-warp (
                                                                                      if (WG_SIZE >= 128) {
        join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 1 \circ
                                                                                         if (tid < 64) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 2 \circ
                                                                                           l data[tid] += l data[tid+ 64]; }
                                                                                        barrier(CLK_LOCAL_MEM_FENCE); }
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 4 \circ
                                                                                      if (tid < 32) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 8 \circ
                                                                                         if (WG SIZE >= 64) {
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 16 \circ
                                                                                           l_data[tid] += l_data[tid+32]; }
       join \circ map-lane (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 32
                                                                                         if (WG SIZE >= 32) {
     ) \circ split 64 \circ
                                                                                           l_data[tid] += l_data[tid+16]; }
     join \circ map-local (reduce-seq (+) 0) \circ split 2 \circ reorder-stride 64 \circ
                                                                                        if (WG_SIZE >= 16) {
     join \circ toLocal (map-local (reduce-seq (+) 0)) \circ
                                                                                           l_data[tid] += l_data[tid+ 8]; }
     split (blockSize/128) o reorder-stride 128
                                                                                         if (WG SIZE >= 8) {
                                                                                           l_data[tid] += l_data[tid+ 4]; }
  ) o split blockSize
                                                                                         if (WG SIZE >= 4) {
                                                                                           l_data[tid] += l_data[tid+ 2]; }
                                                                                         if (WG SIZE >= 2) {
```

```
27
```

l_data[tid] += l_data[tid+ 1]; } }

g_odata[get_group_id(0)] = l_data[0];

if (tid == 0)

Case Study: Matrix Multiplication



```
A x B =
map(λ rowA ↦
map(λ colB ↦
dotProduct(rowA, colB)
, transpose(B))
, A)
```

Tiling as a Rewrite Rules

Naïve matrix multiplication



Register Blocking as a Rewrite Rules









Register Blocking as a Rewrite Rules

$$registerBlocking = Map(f) \Rightarrow Join() \circ Map(Map(f)) \circ Split(k) \\Map(a \mapsto Map(b \mapsto f(a, b))) \Rightarrow Transpose() \circ Map(b \mapsto Map(a \mapsto f(a, b))) \\Map(f \circ g) \Rightarrow Map(f) \circ Map(g) \\Map(Reduce(f)) \Rightarrow Transpose() \circ Reduce((acc, x) \mapsto Map(f) \circ Zip(acc, x)) \\Map(Map(f)) \Rightarrow Transpose() \circ Map(Map(f)) \circ Transpose() \\Transpose() \circ Transpose() \Rightarrow Har \\Reduce(f) \circ Map(g) \Rightarrow Reduce((acc, x) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \circ Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x))) \\Map(f) \otimes Map(g) \Rightarrow Map(f \circ g) \rightarrow f(acc, g(x)) \\Map(f \circ g) \rightarrow f(acc, g(x)) \rightarrow f(acc, g(x)) \\Map(f \circ g) \rightarrow f(acc, g(x)) \rightarrow f(acc, g(x))$$



Heuristics for Matrix Multiplication

For Macro Rules:

- Nesting depth
- Distance of addition and multiplication
- Number of times rules are applied

For Map to OpenCL:

- Fixed parallelism mapping
- Limited choices for mapping to local and global memory
- Follows best practice

For Parameter Mapping:

- Amount of memory used
 - Global
 - Local
 - Registers
- Amount of parallelism
 - Work-items
 - Workgroup

Exploration in Numbers for Matrix Multiplication

Exploration Space for Matrix Multiplication

Only few OpenCL kernel with very good performance

Performance Evolution for Randomised Search

Even with a simple random search strategy one can expect to find a good performing kernel quickly

Performance Results Matrix Multiplication

Performance close or better than hand-tuned MAGMA library

Performance Portability Matrix Multiplication

Generated kernels are specialised for device and input size

Desktop GPUs vs. Mobile GPU

Performance portable even for mobile GPU device!

The LIFT Team

Toomas Remmelg PhD Student University of Edinburgh

-3

aroupSize

48

Node 4

(n = 86137)

2000

000

Performance Modeling of LIFT Programs

Frederico Pizzuti PhD Student University of Edinburgh

Identify hidden parallelism in LIFT programs

Parallelising non-associative reductions

 $x \leftarrow 0$; for i = 0 to n do $x \leftarrow c \cdot x + a[i]$ done.

 $\boldsymbol{x} \leftarrow \boldsymbol{x}_0$; for i = 0 to n do $\boldsymbol{x} \leftarrow A_i \times \boldsymbol{x}$ done,

where
$$\boldsymbol{x} = \begin{pmatrix} x \\ 1 \end{pmatrix}, \ \boldsymbol{x}_0 = \begin{pmatrix} 0 \\ 1 \end{pmatrix}, \ A_i = \begin{pmatrix} c & a[i] \\ 0 & 1 \end{pmatrix}.$$

Key idea: Rearrange data as matrices to exploit associative matrix multiplication

Naums Mogers PhD Student University of Edinburgh

Optimizing Deep Learning with LIFT

Express layers with LIFT primitives

fully_connected(f, weights, bias, inputs) :=
 Map((neuron_weights, neuron_bias) → f() o Reduce(add, neuron_bias) o
 Map(mult) \$ Zip(inputs, neuron_weights)) \$ Zip(weights, bias)

Optimize individual layers and across layers via rewrites

Low Power Devices

Bastian Hagedorn PhD Student University of Münster

Larisa Stoltzfus PhD Student University of Edinburgh

(map([a b c] [d e f] map(map(transpose) • [a b c] map(transpose) • [d e f] slide 2 1 • slide 2 1 • [d e f] [g h i]

Stencil Computations in LIFT

Image Processing

Acoustics Simulation

Video

Explore optimisations as rewrites

Data Parallel Idealised Algol: A New Foundation for LIFT

- Collaboration with Robert Atkey (Strathclyde), Christophe Dubach, and Sam Lindley (Edinburgh)
- More further down the line: formalisation of OpenCL and similar lowlevel models to enforce them via type- and effect-systems

Application of Lift as a code generation backend

Heterogeneous code generation gives a speedup in all cases

Performance close to manual written code —when parallelisation strategy is comparable

Lift is Open-Source Software

http://www.lift-project.org/

https://github.com/lift-project/lift

Iift-project/lift: The Lift program ×					
→ C G GitHub, Inc. [US] https://github.co	om/lift-project/lift			☆ 🛈 📕	fo 📰 🚺 🕸 🏤
C This repository	Search	Pull requests Issues Gist		🌲 +• 👰 •	
📮 lift-project / li	ft		⊙ Unwatch → 7 ★	Star 30 VFork 2	
<> Code (!) Iss	ues 0 11 Pull requests 0	🏴 Projects 0 🗉 Wiki 🥠 P	ulse 🔟 Graphs 🔅 Set	tings	
The Lift programm	ning language http://www.lift-p	roject.org/ — Edit			
🕝 1,923 comm	nits 👂 1 branch	ా o releases	10 contributors	কাঁু MIT	
Branch: master -	New pull request	Creat	e new file Upload files Find f	ile Clone or download -	
🔊 michel-steuwer	michel-steuwer committed on GitHub Made LICENSE file parsable for github Late:		commit 8b13aac 2 days ago		
docker	Cleaning up the to	p folder of the repo and restructuri	ng the docker s	4 months ago	
in highLevel	refactoring			7 months ago	
🖿 lib	Bump ArithExpr			6 days ago	
inative	Add support for qu	uerying if the device supports doub	e	a year ago	
presentations	Added power poin	It slides of ICFP, PL Interest and PE	NCIL meeting.	a year ago	

The *Lift* Project: Performance Portable GPU Code Generation via Rewrite Rules

Michel Steuwer — <u>michel.steuwer@ed.ac.uk</u>

http://www.lift-project.org/

